Amendments to the Specification

In the specification, please replace the paragraph on page 2, lines 7-21, with the following amended paragraph:

U.S. Application No. 09/775,477, filed February 2, 2001, now issued U.S. Patent No. 6,937,538, entitled: Asynchronously Resettable Decoder for a Semiconductor Memory ~~Module with Hierarchical Functionality, Attorney Docket No. 40050/B600/JF0~~; U.S. Application No. 09/776,262, filed February 2, 2001, now issued U.S. Patent No. 6,603,712, entitled: High Precision Delay Measurement Circuit~~, Attorney Docket No. 37079/B600/JFO~~; U.S. Application No. 09/776,220, filed February 2, 2001, now issued U.S. Patent No. 6,492,844, entitled: Single-Ended Sense Amplifier with Sample-and-Hold Reference~~, Attorney Docket No. 37362/B600/JFO~~; U.S. Application No. 09/775,478, filed February 2, 2001, now issued U.S. Patent No. 6,414,899, entitled: Limited Switch Driver Circuit~~, Attorney Docket No. 37361/B600/JFO~~; U.S. Application No. 09/775,476, filed February 2, 2001, now issued U.S. Patent No. 6,724,681, entitled: ~~Fast Decoder with~~ Asynchronous Resettable Decoder with ~~Row~~ Redundancy~~; Attorney Docket No. 37115/B600/JF0;~~ U.S. Application No. 09/776,029, filed February 2, 2001, now issued U.S. Patent No. 6,611,465, entitled: Diffusion Replica Delay Circuit~~, Attorney Docket No. 37360/B600/JFO~~; U.S. Application No. 09/775,475, filed February 2, 2001, now issued U.S. Patent No. 6,535,025, entitled: Sense Amplifier with Offset Cancellation and Charge-Share Limited Swing Drivers~~, Attorney Docket No. 37363/B600/JF0~~; U.S. Application No. 09/775,701, filed February 2, 2001, now issued U.S. Patent No. 6,411,557, entitled: Memory Architecture with Single-Port Cell and Dual-Port (Read and Write) Functionality~~, Attorney Docket No. 37364/B600/JFO~~; U.S. Application No. 09/776,263, filed February 2, 2001, now issued U.S. Patent No. 6,745,354, entitled: Memory Redundancy Implementation~~, Attorney Docket No.~~

~~37496/B600/JFO~~; and U.S. Application No. 09/776,028, filed February 2, 2001, now issued U.S. Patent No. 6,417,697, entitled: A Circuit Technique for High Speed Low Power Data Transfer Bus~~, Attorney Docket No. 37497/B600/JFO~~.